Excellent charge offset stability in a Si-based single-electron tunneling transistor

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We have measured the long-term drift and the short-term $1/f$ noise in the charge offset $Q_0(t)$ in two Si-based single-electron tunneling transistors (SETTs). In contrast to metal-based SETTs, these devices show excellent charge stability, drifting by less than $0.01e$ over weeks. The short-term $1/f$ noise magnitude is similar to the metal-based devices, demonstrating that different mechanisms are responsible for the short-term noise versus the long-term drift. Finally, we show that, in addition to the excellent stability over time, it may be possible to make the devices more robust with respect to voltage-induced instability as well. © *2001 American Institute of Physics.*
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Single-electron tunneling (SET) devices have been proposed as one possible candidate for future microelectronics, after complementary metal–oxide–semiconductor (CMOS) technology reaches its limits.[1] SET devices are based on the "Coulomb blockade,"[2] which refers to the physical phenomenon that occurs when the energy to charge a conductor with *one additional electron* becomes a significant impediment to charge transfer.

In SET transistors (SETTs), we have the capability to monitor the motion of fractions of one electron; in SET pumps, we can *control* the motion of single electrons. In addition to microelectronics applications, this capability has excited interest in the electrical metrology (study of standards) community, for the obvious reason that it offers the potential to produce standards based on the charge of one electron, in particular a standard for capacitance[3] or current.

The fact that SET devices are sensitive to the motion of single electrons is both a great advantage (SETTs are by far the world's best charge electrometers, allowing sensitivity at or below $10^{-3}e$)[3] and a great disadvantage (because of the "charge offset" problem). The charge offset refers to the fact that there is a random offset to the correct operation gate voltage for SET transistors or pumps; this random offset is due to trapped, possibly mobile, charges in the defected material near the SET device.

As an example, we show the transistor control curve in the inset of Fig. 1; it shows the modulation of the source–drain current I_{S-D} with gate voltage $\mathcal{V}_G$ measured on one of our Si-based SETTs. The period of this modulation corresponds to a change of the SET island charge $\Delta Q_0 = C_G \Delta \mathcal{V}_G = 1e$. The charge offset adds a random phase offset to this periodic modulation; if the offset is a substantial fraction of $1e$ or greater, it will change the operation of the device, thus making it useless.

There have been a number of reports of the time-dependent charge offset noise in *metallic* SETTs due to mo-

tion of the trapped defect charges; most of these reports have concentrated on the $1/f$ noise at frequencies at or above about 0.01 Hz.[4–7] Such measurements are important for SETT use as a charge electrometer; for example, the $1/f$ noise sets the resolution limit of the electron-counting capacitance standard.[3]

However, these measurements do not yield information on the rare large charge offset changes which can change operation. This can be seen by a simple argument: a simple estimate shows that a typical $1/f$ charge noise, with amplitude $10^{-3}e/\mathrm{Hz}^{1/2}$, can only produce a offset change of $\Delta Q_0 = 1e$ after many years. Thus, the rare changes of Q_0 by a large fraction of e cannot be attributed to low frequency extrapolation of the $1/f$ noise measured at higher frequencies.

This has impelled us to measure the "long-term drift" of the charge offset in SET devices in order to examine those rare large changes in Q_0 which are the only ones important to gross device operation. In metal-based devices, such events are fairly common, occurring within the thermal cycle or, for a quiescent device, within typically a few days.[8,9] We have shown that attempts at a variety of material and geometry solutions have been unsuccessful in alleviating this problem.[8]

Again, a simple argument shows the importance of this long-term drift: a conservative attempt at an integrated device would require 10^3 devices, with a 10^{-4} probability that any of the devices would drift from their correct operating conditions enough to invalidate the operation. A simple estimate shows that for metal-based devices similar to the ones we have tested previously, if all devices start off correctly tuned, these criteria would be violated (one or more devices would drift too far) within about 0.02 s; this is unacceptable for many applications, including metrological ones.

More recently, the capability to make controllable SET devices based on silicon-on-insulator (SOI) devices has been demonstrated.[10] In particular, we reported that there was no change in the charge offset with thermal cycling in these

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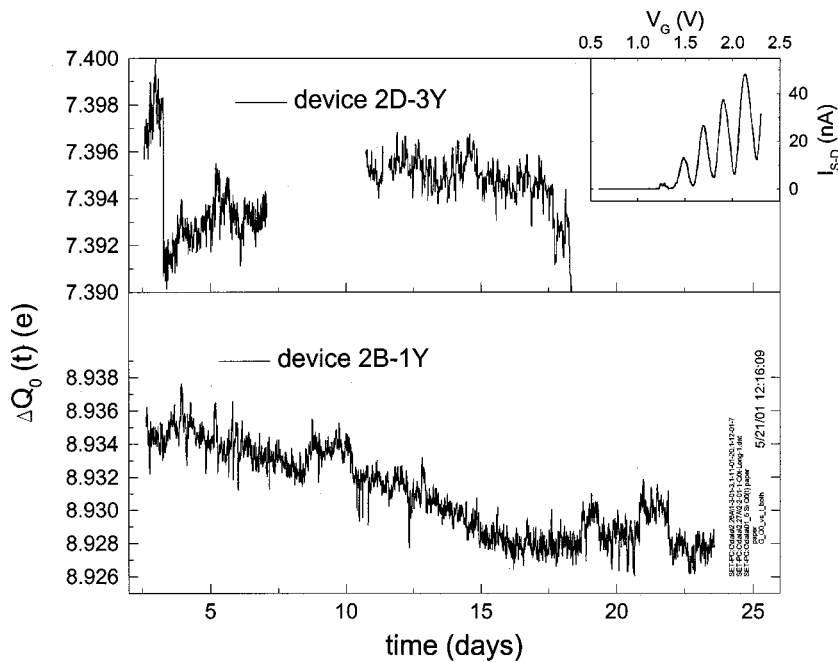
FIG. 1. Inset: Source–drain current as a function of the front gate voltage, showing the typical periodic modulation. Each period corresponds to changing Q_0 by $1e$. Top: Measurement of the long-term drift in $Q_0(t)$ as a function of time. The first day was at a temperature $T < 0.1$ K; the other days it was at 4 K. This shows the insensitivity of $Q_0(t)$ to temperature. Bottom: Longer measurement in a second device, with different geometry, on a different die. Both devices show excellent stability: $\Delta Q_0(t) < 0.01e$.

devices.[10] Impelled by this finding, we have performed, and report herein, long-term drift measurements of two of our Si SETTs. In contrast to the metal-based devices, we have found an excellent charge offset stability, with a drift of less than $0.01e$ over many days of measurement.

There have been many measurements of noise due to charge traps and, in particular, of "random telegraph signals" (RTSs) in small metal–oxide–semiconductor field-effect transistors (MOSFETs).[11] These studies have shown that there can be many charge traps in Si-based devices, whose trapping and emission can modulate the I_{S-D} in MOSFETs. In addition, one study[12] of single-electron dots in highly doped Si reported a large change in charge offset, with a concomitant increase in time-dependent noise. A second study[13] reported similar results in a similar device. We note that these devices were made without deliberate tunnel junctions, suggesting that the spatial potential modulation due to defects is crucial in forming the SETT.[14] In turn, we suspect that this suggests that these devices will intrinsically be more susceptible to charge offset problems than devices in which the tunnel junctions are deliberately formed as in the devices reported herein.

The SET transistors reported herein were fabricated using our standard technique of pattern-dependent oxidation (PADOX);[10,15] in brief, this process starts with a SOI lightly doped wafer, after which a short, narrow line of Si is formed between two larger pads. Gate oxidation then forms two tunnel junctions where the wire widens out to the pads, with a SET island in the middle of the wire. We then deposited high-temperature oxide, followed by poly-Si gate and self-aligned ion implantation for the source and drain.

We measured the charge offset drift as a function of time in two ways: for crude measurements (with an uncertainty of about $0.005e$), we repeatedly measured the gate voltage dependence of the source–drain voltage $I_{S-D}(\mathscr{V}_G)$, and monitored the possible change over time of a particular feature in the $I_{S-D}(\mathscr{V}_G)$. For the finer measurements in Fig. 1, we used a simple feedback circuit by applying a square wave to $\mathscr{V}_G$,

and using the output of a lock-in amplifier to maintain a peak in $I_{S-D}(\mathscr{V}_G)$ at the same point. Then, by monitoring the feedback voltage, we can monitor Q_0 with a noise floor of about $10^{-4}e$.

The main part of Fig. 1 shows long-term drift $Q_0(t)$ while holding the source–drain voltage fixed at 20 mV (all results in this letter were insensitive to gate voltages or magnetic fields up to 5 T, and only weakly sensitive to the source–drain voltage). Figure 1 shows the basic result of this letter: unlike our results in metal-based SETTs,[8] *the charge offset in this Si-based SETT drifted by less than* $0.006e$ *over about 15 days*. In the upper half, the hysteretic change at the beginning shows that the charge offset changed by about $0.006e$ between temperatures of 4.2 K and much lower (less than 0.1 K). Similar measurements in a second device in the lower half of Fig. 1 (different die, different gate capacitance) showed a total deviation of $0.008e$ over 21 days. Also, two individual (not continuous) measurements on a third device (not shown) separated by 7 years showed a change of $0.04e$.

Figure 2 shows the power spectral density measured over two decades of frequency from the time dependence of the current $I_{S-D}(t)$. We see that the power spectral density has the typical "colored" spectrum: $S(f)$ rises as f decreases. The absolute magnitude has a value that is typical of other (metal-based) SETTs,[4,6] whereas the long-term drift in the Si-based devices is about 1000 times smaller. This again demonstrates the point made above: $1/f$ noise does not arise from the same mechanism as that which causes the large ΔQ_0 changes in metal-based SETTs.[9]

The excellent results for the $Q_0(t)$ in these Si-based devices suggest one further question: What can cause Q_0 to change by a large amount? It is well known that noise-producing defects in many small devices can be produced/destroyed/controlled by a voltage pulse. We have attempted a preliminary study of this in our devices as follows. We have made periodic crude measurements of $Q_0(t)$, while applying voltage pulses in various ways. First of all, we have found that pulses up to 20 mV applied to the source/drain
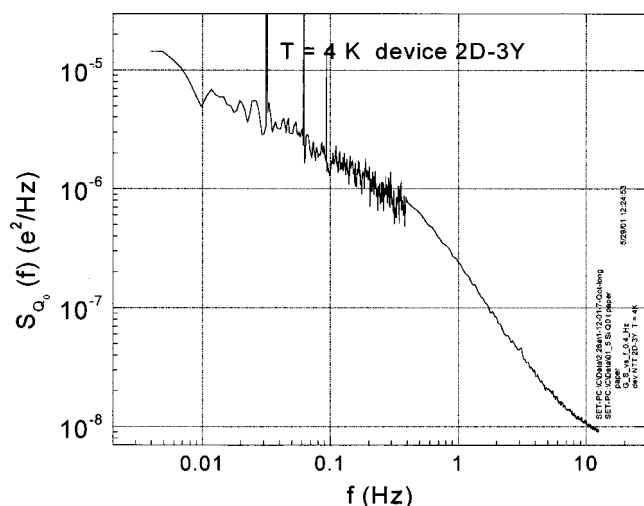
FIG. 2. Power spectral density of charge offset fluctuations as a function of the frequency. The measurements above and below 0.01 Hz were made differently (see text). While the long-term drift in Fig. 1 is orders of magnitude better than that in metal-based devices, the $1/f$ noise shown here is similar in magnitude to that in metal-based ones.
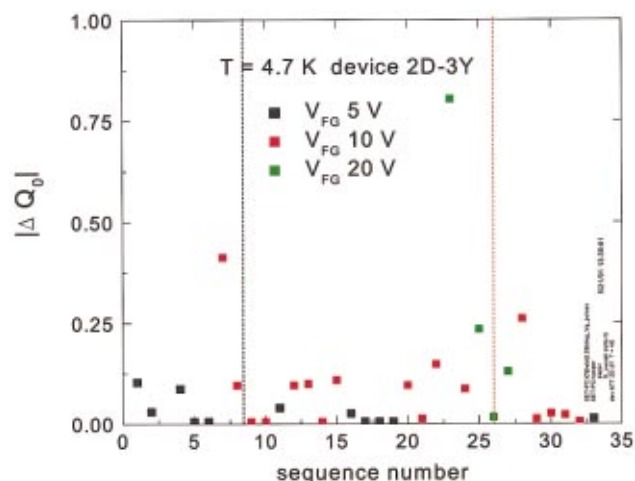

FIG. 3. (Color) Absolute magnitude of hysteretic charge offset changes as a function of the front gate voltage pulse that caused it. Note that the changes from ± 5 V (black squares) are much smaller after the first ± 10 V pulse (to the right of the black line). Note the similar change in ± 10 V (red) after the first ± 20 V (red line). These suggest that the Si-based SETT can be made insensitive to such voltage-induced instabilities.

had no effect; also, voltages applied to the back gate of up to 60 V (corresponding to $\Delta Q_0 \approx 0.13e$) also had no effect, while 90 V may have caused a ΔQ_0 as large as $0.06e$.

Finally, we performed measurements while pulsing the front gate. We found that: (1) hysteretic changes in Q_0 were possible, but only occurred instantaneously (i.e., no subsequent drift over time, with a minimum resolution of a few minutes); (2) the type of pulsing (slow sweep, square wave at 1 kHz, square wave at about 1 Hz) was unimportant; (3) the response of Q_0 to repeated pulses could be "trained" out.

To demonstrate this last point, we show in Fig. 3 the hysteretic Q_0 changes measured after pulses of ± 5, 10, or 20 V (corresponding to ΔQ_0 of about 20, 40 or $80e$). In general, it is clear that voltage pulses can cause hysteretic Q_0 changes. However, careful examination suggests that *the application of a larger pulse renders the device much less sensitive to the smaller pulses*. For instance, after the first 10 V pulse (to the right of the black vertical line), the size of the 5 V changes (black squares) was generally smaller. Similarly, the size of the 10 V changes is substantially smaller after the first 20 V pulse. Although by no means conclusive, Fig. 3 indicates that a more comprehensive engineering study could suggest processes that could make the SETT insensitive to such voltage-induced shocks.

To summarize, we have measured the time-dependent drift of the charge offset $Q_0(t)$ in Si-based SET transistors. The lack of drift indicates that these devices are far better than the metal-based SETTs we have already studied. Although the long-term drift is much better, the short-term $1/f$ noise is similar to that of the metal-based SETTs, again dem-

onstrating the different mechanisms responsible for the two. Also, we have found strong indications that the sensitivity to large voltage pulses can be trained out of the devices. Finally, these two questions naturally arises: What is the cause of the improvement of Si-over metal-based SETTs and are all Si-based SET devices this good? We plan on studying this next, by examining Si-based SET devices fabricated using different schemes; these devices will have deliberately formed tunnel junctions, in contrast to the studies referenced at the beginning of this letter.[12,13]

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